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METHOD FOR ETCHING A SEMICONDUCTOR SUBSTRATE USING GERMANIUM HARD MASK

Field of the Invention

The present invention relates, in general, to semiconductor device fabrication and, more particularly, to etching processes used in the fabrication of semiconductor devices.

Background of the Invention

Etching is widely used in the fabrication of semiconductor devices. A process for etching a pattern, e.g., a trench, in a semiconductor substrate usually starts with forming a mask on the substrate. The substrate is then etched through the mask, which defines the pattern etched in the substrate. Photo resist is typically used for forming the mask. In some processes, e.g., deep trench etching, the etch selectivity to the photo resist material is insufficient, and the etching process depletes the photo resist mask and damages the underlying substrate.

In such etching processes, a dielectric hard mask, e.g., a thick silicon dioxide or silicon nitride hard mask, can be used to effectively protect the underlying substrate. Patterning a thick dielectric hard mask requires a thick photo resist mask. However, forming small patterns in a thick photo resist mask is difficult because of the shrinking photolithography depth of focus. Thus, such etching processes are not suitable for fabricating high density and high performance semiconductor devices. In addition, silicon dioxide and silicon nitride are commonly used to form dielectric structures over a semiconductor substrate. Thus, removing the hard mask after the etching process often alters and/or damages the dielectric structures underlying the hard mask. This may adversely affect the performance, characteristics, and reliability of the semiconductor devices fabricated on the substrate. The dielectric hard mask can also be patterned using a silicon mask deposited thereon. However, the removal of the silicon

mask often alters and damages the underlying semiconductor substrate, thereby adversely affecting the performance of the semiconductor devices fabricated thereon.

Accordingly, there exists a need for a process for etching a semiconductor substrate using a hard mask that does not adversely affect the performance, characteristics, and reliability of the semiconductor devices fabricated on the semiconductor substrate. More particularly, it is desirable to be able to remove the hard mask without affecting the underlying material on the semiconductor substrate. It is also desirable for the etching process to be simple and cost efficient. It would be of further advantage for the etching process to be compatible with existing semiconductor device fabrication processes and suitable of fabricating high performance semiconductor devices.

Summary of the Invention

A general advantage of the present invention is providing a process for etching a semiconductor substrate using a hard mask that does not adversely affect the performance, characteristics, and reliability of the semiconductor devices fabricated on the semiconductor substrate. A specific advantage is that the process of removing the hard mask does not alter and/or damage the underlying structure on the semiconductor substrate. Another specific advantage of the present invention is that the etching process is suitable for fabricating high density and high performance semiconductor devices. A further advantage is that the etching process is simple and cost efficient. An additional advantage of the present invention is that the etching process is compatible with existing semiconductor device fabrication processes.

These and other advantages of the present invention are achieved through using a germanium hard mask in an etching process. In accordance with the present invention, the etching process includes forming a dielectric layer over a major surface of a semiconductor substrate and depositing a thin layer of metallic germanium over the dielectric layer. The layer of metallic germanium is patterned to form the germanium hard mask. The dielectric layer is selectively etched through the germanium hard mask to form a pattern over the semiconductor substrate, which is etched using the dielectric

layer pattern as a mask.

Patterning the thin metallic germanium layer is preferably achieved using a thin mask, e.g., a thin photo resist mask. Because of their compatibility with shallow depth of focus photolithography processes, thin photo resist masks are preferred in the fabrication of semiconductor devices with small features. Therefore, the etching process of the present invention is suitable for fabricating high density and high performance semiconductor devices. The removal of the germanium hard mask can be easily achieved by oxidizing the metallic germanium hard mask to transform it into a layer of germanium oxide and rinsing the semiconductor substrate in water to remove the germanium oxide layer. Germanium oxidation and water rinse have minimum effects on the semiconductor substrate. Therefore, the etching process of the present invention does not adversely affect the performance, characteristics, and reliability of the semiconductor devices fabricated on the semiconductor substrate. In a preferred embodiment, the germanium hard mask is removed before etching the semiconductor substrate to further protect the semiconductor devices fabricated thereon from any possible adverse effect.

Brief Description of the Drawings

FIGs. 1-6 are schematic cross sectional views of a semiconductor substrate at various stages of an etching process in accordance with the present invention.

It should be noted that the figures are merely schematic representations, which are not intended to portray specific parameters of the present invention. The figures should not be considered as limiting the scope of the present invention. In addition, the figures are not drawn to scale. Elements having similar functions are labeled using the same reference numerals in the figures.

Detailed Description of the Preferred Embodiments

Generally, the present invention provides an etching process using a germanium hard mask. The germanium hard mask is formed by patterning a metallic germanium layer deposited over a dielectric layer disposed over a semiconductor substrate. Through the germanium hard mask, the dielectric layer is selectively etched to form a pattern over the semiconductor substrate, which is etched using the dielectric layer pattern as a mask. The patterning of the metallic germanium layer is preferably achieved using a thin mask, e.g., a thin photo resist mask. The germanium hard mask is stripped away through germanium oxidation and water rinse, both of which have minimum effects on the semiconductor substrate. In a preferred embodiment, the germanium hard mask is oxidized and rinsed away before etching the semiconductor substrate.

FIG. 1 is a schematic cross sectional view of a semiconductor substrate 10 at an early stage of an etching process in accordance with the present invention. Typically, semiconductor substrate 10 shown in FIG. 1 is a part of a semiconductor wafer. By way of example, semiconductor substrate 10 is a bulk silicon substrate. However, it should be noted that the etching process of the present invention is also applicable in etching other types of substrates such as, for example, silicon <u>s</u>emiconductor <u>o</u>n <u>i</u>nsulator (SOI) substrates, silicon carbide substrates, gallium arsenide (GaAs) substrates, silicon germanium substrates, ceramic substrates, etc. Substrate 10 has a major surface 11. A layer 12 of silicon dioxide having a thickness between approximately 5 <u>n</u>ano<u>m</u>eters (nm) and approximately 30 nm is disposed on major surface 11 of substrate 10. Layer 12 serves to protect major surface 11 of substrate 10 in a process of fabricating semiconductor devices (not shown) on substrate 10 and is also referred to as a pad oxide layer. A silicon nitride layer 14 having a thickness between approximately 50 nm and approximately 300 nm and a silicon dioxide layer 16 having a thickness between approximately 800 nm and approximately 3000 nm are disposed over layer 12 of pad oxide. Silicon dioxide layer 16 is also referred to as a mask oxide layer. Pad oxide layer 12, silicon nitride layer 14, and silicon dioxide layer 16 are also referred to as dielectric layers. Techniques for forming dielectric layers 12, 14, and 16 include oxidation, deposition, etc., which are well known to those skilled in the art. Dielectric

layers 12, 14, and 16 form a dielectric stack 15 over major surface 11 of substrate 10. It should be noted that dielectric stack 15 is not limited to including three dielectric layers 12, 14, and 16 as shown in FIG. 1. In accordance with the present invention, dielectric stack 15 can includes any number of dielectric layers, e.g., one, two, four, five, etc. Further, the thickness of each layer in dielectric stack 15 is not limited to those described above. It can vary to optimize the fabrication process and devices performance.

Referring now to FIG. 2, a layer 22 of metallic germanium is deposited over dielectric stack 15. By way of example, layer 22 of metallic germanium has a thickness between approximately 40 nm and approximately 500 nm and is deposited over dielectric stack 15 in a chemical vapor deposition process. A photo resist layer 24 is deposited over metallic germanium layer 22. Using exposing and developing techniques known in the art, photo resist layer 24 is patterned to form a photolithography image over metallic germanium layer 24. In other words, a photo resist photolithography mask is formed over layer 22 of metallic germanium.

Next, metallic germanium layer 22 is etched through the photolithography image formed by photo resist layer 24. A reactive ion etching (RIE) process is preferably used to etch metallic germanium layer 22. Other etching process having a high etch selectivity between metallic germanium and photo resist can also be used to etch metallic germanium layer 22 through the mask formed by photo resist layer 24. Because of high the etch selectivity of metallic germanium relative to photo resist, photo resist layer 24 can be a thin layer of photo resist material. The thickness of photo resist layer 24 can further reduced by using a thin layer 22 of metallic germanium, thereby shortening the metallic germanium etching process. A thin photo resist mask is compatible with a shallow depth of focus photolithography processes, and therefore is preferred in the fabrication of semiconductor devices with small features. After etching layer 22 of metallic germanium, photo resist layer 24 is stripped away using techniques known in the art. The remaining germanium serves as a metallic germanium hard mask 25 over of dielectric stack 15 as shown in FIG. 3. Germanium hard mask 25 has openings, e.g., openings 26 shown in FIG. 3, through which dielectric stack 15 is selectively etched in a subsequent step of the etching process.

Referring now to FIG. 4, silicon dioxide layer 16, silicon nitride layer 14, and

pad oxide layer 12 in dielectric stack 15 are etched through germanium hard mask 25. By way of example, an RIE process is used to etch dielectric stack 15. It should be noted that dielectric layers 16, 14, and 12 in dielectric stack 15 can be etched either in a single RIE step or in several successive RIE steps, one step for etching each of dielectric layers 16, 14, and 12. The RIE process is preferably highly selective to germanium hard mask 25 so that germanium hard mask 25 will not be depleted during the etching process. After etching, dielectric stack 15 forms a dielectric hard mask 35 over major surface 11 of substrate 10. Portions of major surface 11 of substrate 10 are exposed through openings 36 in dielectric hard mask 35.

Metallic germanium hard mask 25 is preferably stripped away after forming dielectric hard mask 35. In a preferred embodiment, layer 22 of metallic germanium is oxidized and transformed into a layer 27 of germanium oxide as shown in FIG. 5. The oxidation of metallic germanium layer 22 can be achieved by placing substrate 10 in an environment of elevated temperature with ambient oxygen. In a preferred embodiment, the germanium oxidation is achieved in an anodic oxidation process, in which an electric bias is applied on metallic germanium layer 22. The time duration of the anodic oxidation process depends on the thickness of metallic germanium layer 22, the applied bias, and the temperature of substrate 10 during the oxidation process. For example, in one anodic oxidation process, a bias of approximately fifty volts is applied to metallic germanium layer 22 and semiconductor substrate 10 is placed at a temperature between approximately 500 degrees Celsius (°C) and approximately 600 °C. The oxidation process lasts between approximately fifteen minutes and approximately 60 minutes.

After oxidation, germanium oxide layer 27 can be removed or stripped from substrate 10 by rinsing substrate 10 or the semiconductor wafer that includes substrate 10 with water. After germanium oxide layer 27 is stripped from the top of dielectric stack 15 over substrate 10, dielectric stack 15 serves as dielectric hard mask 35 (shown in FIG. 6) for subsequently etching semiconductor substrate 10. To form semiconductor devices (not shown) such as, for example, field effect transistors, bipolar transistors, etc., on semiconductor substrate 10, other processing steps are performed after etching semiconductor substrate 10 through dielectric hard mask 35. These steps include, but are not limited to, forming doped regions in semiconductor substrate 10 through implantation and/or diffusion; forming dielectric structures over semiconductor

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substrate 10 through oxidation, deposition, and etching; and forming conductive structures over semiconductor substrate 10. These and other process steps for forming semiconductor devices on substrate 10 are known to those skilled in the art.

Using dielectric hard mask 35 in etching semiconductor substrate 10 is compatible with forming deep trenches in semiconductor substrate 10. More particularly in a deep trench etching process, a thick dielectric hard mask like dielectric hard mask 35 shown in FIG. 6 is not prone to be depleted and, therefore, effectively protects the underlying surface of the substrate like major surface 11 of semiconductor substrate 10. In accordance with the present invention, dielectric hard mask 35 is formed by selectively etching dielectric stack 15 through thin metallic germanium hard mask 25 (shown in FIG. 4). This is achievable due to the high etch selectivity of metallic germanium with respect to dielectric materials such as silicon dioxide and silicon nitride. A thin germanium hard mask can be formed using a thin photo resist mask, thereby making the etching process of the present invention suitable for shallow focal depth photolithography processes.

A preferred way of removing metallic germanium hard mask 25 is converting metallic germanium into germanium oxide and rising away the germanium oxide with water. Germanium oxidation and water rinse has minimum adverse effects on the structures formed on semiconductor substrate 10. In accordance with the present invention, the removal of germanium hard mask 25 can be performed either before etching substrate 10 through dielectric hard mask 35 or at a later stage in the semiconductor device fabrication process. In a preferred embodiment, germanium hard mask 25 is removed after etching dielectric stack 15 to form dielectric hard mask 35 and before etching substrate 10 through dielectric hard mask 35. This approach further minimizes any possible effect of the etching process on the semiconductor devices formed on substrate 10.

By now it should be appreciated that a process for etching a semiconductor substrate has been provided. In accordance with the present invention, the etching process includes depositing a thin layer of metallic germanium on a dielectric layer disposed over a major surface of the semiconductor substrate. The metallic germanium layer is patterned to form a germanium hard mask. The dielectric layer is selectively etched through the germanium hard mask to form a dielectric hard mask over the

semiconductor substrate, which is subsequently etched through the dielectric hard mask. The germanium hard mask can be easily removed or stripped away by oxidizing the metallic germanium hard mask to transform it into a layer of germanium oxide and rinsing the semiconductor substrate in water. Thus, the removal process of the germanium hard mask has minimum effects on the semiconductor substrate. In a preferred embodiment, the germanium hard mask is removed before etching the semiconductor substrate to further protect the semiconductor devices to be fabricated thereon from any possible adverse effect. The thin metallic germanium layer can be patterned using a thin mask, e.g., a thin photo resist mask, which is preferred in the fabrication of semiconductor devices with small features. Therefore, the etching process of the present invention is suitable for fabricating high density and high performance semiconductor devices. In addition, the etching process of the present invention is that the etching process is simple, cost efficient, and compatible with existing semiconductor device fabrication processes.